

**Notice of References Cited**

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Applicant(s)/Patent Under  
Reexamination  
KALOGEROPOULOS, SPIROS

Examiner

Mary J. Steelman

Art Unit

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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,367,651	11-1994	Smith et al.	717/149
*	B	US-5,557,797	09-1996	Yano, Takanori	717/124
*	C	US-5,946,491	08-1999	Aizikowitz et al.	717/158
*	D	US-5,950,009	09-1999	Bortnikov et al.	717/158
*	E	US-6,269,477 B1	07-2001	Fitzgerald et al.	717/131
*	F	US-6,175,957 B1	01-2001	Ju et al.	717/156
*	G	US-6,817,013 B2	11-2004	Tabata et al.	717/151
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chen, Gang; Smith, Michael D; "Reorganizing Global Schedules for Register Allocation", p. 408-416, Harvard Publication 1999, retrieved from google.com search <URL www.eecs.harvard.edu/bube/publications/ics99.pdf> on 01/06/2005.
	V	Freudenberger, Stefan M; Gross, Thomas R; Lowney, P. Geoffrey; "Avoidance and Suppression of Compensation Code in a Trace Scheduling Compiler", p. 1156-1214, ACM 1994, retrieved 01/06/2005.
	W	Goodman, James R; Hsu, Wei-Chung, "Code Scheduling and Register Allocation in Large Basic Blocks", p. 442-452, 1988 ACM, retrieved 01/06/2005.
	X	Norris, Cindy; Pollock, Lori L; "An Experimental Study of Several Cooperative Register Allocation and Instruction Scheduling Strategies", p. 169-179, 1995 IEEE, retrieved 01/06/2005.

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.